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ABSTRACT:

The object of this invention is to plan to generalize high speed signal interface unit means of a synchronous optical multiplexing station. The synchronous optical multiplexing station has the transmission unit 100 composed of the buffer memory unit 101, the multiplexing unit 102, the overhead insertion unit 103, the optical transmission unit 104 and the first variable delay unit 105, and the receiving unit 200 composed of the optical receiving unit 210, the frame synchronization unit 220, the overhead termination unit 230, the demultiplexing unit 240, the pointer processing unit 250 and the second variable delay unit 260, and the clock distribution unit 2. And the synchronous optical multiplexing station is comprised to enable to vary the read frame phase of the transmission side buffer memory unit in the high speed signal interface unit and the read frame phases of the receiving side pointer processing unit by varying the reference clock and frame in the station inputted from the clock distribution unit 2 using the amount of delay of the first variable delay unit 105 and the second variable delay unit 260.

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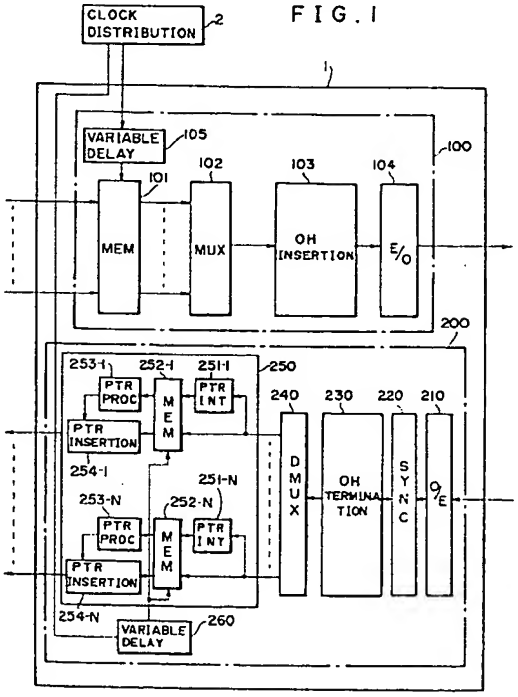
(54) A synchronous optical multiplexing system.

(57) The object of this invention is to plan to generalize high speed signal interface unit means of a synchronous optical multiplexing station.

The synchronous optical multiplexing station has the transmission unit 100 composed of the buffer memory unit 101, the multiplexing unit 102, the overhead insertion unit 103, the optical transmission unit 104 and the first variable delay unit 105, and the receiving unit 200 composed of the optical receiving unit 210, the frame synchronization unit 220, the overhead termination unit 230, the demultiplexing unit 240, the pointer processing unit 250 and the second variable delay unit 260, and the clock distribution unit 2. And the synchronous optical multiplexing station is comprised to enable to vary the read frame phase of the transmission side buffer memory unit in the high speed signal interface unit and the read frame phases of the receiving side pointer processing unit by varying the reference clock and frame in the station inputted from the clock distribution unit 2 using the amount of delay of the first variable delay unit 105 and the second variable delay unit 260.

FIG. 1



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This invention relates to a synchronous optical multiplexing system having an STM-m (STM: Synchronous Trasport Module signal of CCITT Recommendation G.708) low speed electric signal interface according to the SDH standard in the station, and transmitting an STM-n (n = N x M) optical signal multiplexing the STM-m signals.

Conventionally, this kind of high speed signal interface (Fig.1, 2) of synchronous optical multiplexing station has been comprised of the transmission unit 100 and receiving unit 200. The trasmission unit 100 comprises the buffer memory unit 101 to align phases of N STM-m electric signals from a slow speed signal interface unit and read by a clock and frame in the station, the multiplexing unit 102 to multiplex N STM-m electric signals outputted from the buffer memory unit to an STM-n electric signal according to a multiplexing rule of the SDH, the overhead insertion unit 103 to insert an overhead into the STM-n signal outputted from the multiplexing unit, and the optical transmission unit 104 to convert the STM-n electric signal in which the overhead is inserted to an STM-n optical signal and transmit it to a transmission path. The receiving unit 200 comprises the optical receiving unit 210 to convert the STM-n optical signal received from the transmission path to the STM-n electric signal, the frame synchronization unit 220 performing a frame synchronization with the STM-n electric signal, the overhead termination unit 230 to terminate the overhead of the frame-synchronized output signal of the frame synchronization unit, the demultiplexing unit 240 to demultiplex a signal outputted from the overhead termination unit into N STM-m electric signals, the pointer processing unit 250 to move N STM-m signals from a transmission path clock and frame onto a clock and frame in the station and modify pointer information to show the practical leading portion of the data within the STM-m signals to a value aligned to the frame in the station and send out the signals to a low speed signal interface unit in the station as N STM-m electric signals.

At the buffer memory unit 101 in the transmission unit, to reduce the memory capacity, corresponding to the frame phase of the STM-m signals inputted from the low speed signal interface unit, the frame pulse inputted from the clock distribution unit 2 used as the read frame is fixedly given a delay and the write and read frames are aligned. In addition, at the pointer processing unit 250 of the receiving unit, the read frame phase is fixed by the phase decided based on the frame inputted from the clock distribution unit 2.

The reason why the low speed side electric signal interface is the SDH standard is to improve expansibilities of the station by standardizing the interface. However, the input/output frame phase of the low speed electric signal observed from the high speed signal interface unit may be changed due to the difference of the station's structures, that is the difference of the circuits which are connected to the buffer memory unit 101 and the pointer processing unit 250. If the read frame phases of the buffer memory unit 101 and the pointer processing unit 250 are fixed as a conventional embodiment, there is a problem that the high speed signal interface unit can not be used in the different station, although it can be used in the same station.

The object of this invention is to plan to generalize the high speed signal interface unit by setting the read frame phases of the high speed signal interface unit transmission side buffer memory unit and the receiving side pointer processing unit to be variable.

The synchronous optical multiplexing station of this invention comprises a transmission unit for multiplexing M STM-m low speed signals of the SDH standard to an STM-n (n = N x m) high speed signal, and a receiving unit demultiplexing an STM-n high speed signal to N STM-m low speed signals, and to achieve the above-mentioned object includes:

transmission unit having:

buffer memory unit means for aligning phases of N STM-m electric signals outputted from a slow speed signal interface unit and reading by a clock and frame in the station;

the first variable delay unit means for optionally varying a read frame phase of the buffer memory unit means for one frame by setting from outside with the frame phase of the STM-m electric signals inputted from the low speed signal interface unit;

multiplexing unit means for multiplexing N STM-m electric signals outputted from the buffer memory unit means to the STM-n electric signal according to the multiplexing rule of the SDH;

overhead insertion unit means for inserting an overhead into the STM-n signal outputted from the multiplexing unit means; and

optical transmission unit means for converting the STM-n electric signal in which the overhead is inserted to an STM-n optical signal and transmitting it to a transmission path;

said receiving unit having:

an optical receiving unit means for converting the STM-n optical signal inputted from the transmission path to the STM-n electric signal;

frame synchronization unit means for frame-synchronizing the STM-n electric signal;

overhead termination unit means for terminating the overhead of the frame-synchronized output signal of the frame synchronization unit means;

demultiplexing unit means for demultiplexing sig-

nals outputted from the overhead termination unit means to N STM-m electric signals;
pointer processing unit means for moving N STM-m signals from a transmission path clock and frame onto a clock and frame in the station, and modifying pointer information to show the practical leading point of the data within the STM-m signals to a value aligned to the frame in the station and sending out the signals to a low speed signal interface unit in the station as N STM-m electric signals;
the second variable delay unit means for optionally varying a frame phase for one frame by setting from outside at moving the clock and frame in the pointer processing unit means.

More, it is preferable that delay quantities of the first and second variable delay units means are set by receiving a control signal from outside through a control interface.

More, it is preferable that delay quantities of the first and second variable delay units means are set by inserting an identification information into the STM-m low speed signals by the slow speed signal interface unit, and detecting and identifying this at the high speed signal interface unit.

Further more, it is preferable that the pointer processing unit means is equipped with a pointer interpretation unit, a memory unit, a pointer operation unit, and a pointer insertion unit.

The invention has such an effect that it is made possible to optionally decide the read frame phase of the buffer memory for aligning a phase of N low speed signal in an input device of the high speed signal interface unit transimission side and the read frame phase of the receiving side pointer processing unit by setting of delay quantity of the variable delay unit, so that it becomes possible to use the same high speed signal interface unit and generalize the high speed signal interface unit, even though the low speed STM-m electric signal input/output frame phase of the high speed signal interface unit is differentiated by the various station's configuration.

Fig.1 illustrates a block diagram showing an embodiment of this invention.

Fig.2 illustrates a block diagram showing a conventional high speed interface unit of the synchronous signal multiplexing unit

Fig.3 illustrates a chart which shows a format of an STM-1 signal.

Fig.4 illustrates a block diagram showing a pointer processing unit 250 in the embodiment shown in Fig.1.

Fig.5, Fig.6 and Fig.7 illustrate charts to explain the pointer processing unit shown in Fig.4.

Fig.8 illustrates a block diagram showing an embodiment when controlling the variable delay unit from outside.

Fig.9 illustrates a block diagram showing an embodiment when controlling the variable delay unit automatically.

Next, the invention is described referring to following figures. Fig.1 is a block diagram showing the embodiment of the invention.

A synchronous optical multiplexing station by this invention includes the high speed signal interface unit 1 consisting of the transmission unit 100 comprising the buffer memory unit 101, the multiplexing unit 102, the overhead insertion unit 103, the optical transmission unit 104, and the first variable delay unit 105, and the receiving unit 200 comprising the optical receiving unit 210, the frame synchronization unit 220, the overhead termination unit 230, the demultiplexing unit 240, the pointer processing unit 250 and the second variable delay unit 260, and the clock distribution unit 2 distributing the reference clock and the frame pulse in the station into the station.

At the transmission unit 100 the phases of N STM-1 low speed electric signals inputted at the buffer memory unit 101 are aligned, and the N STM-1 signals are multiplexed to the STM-n signal according to the multiplexing rule of the CCITT Recommendation G.708 at the multiplexing unit 102, and the overhead is inserted into the signal at the overhead insertion unit 103 and it is converted into the STM-n optical signal at the optical transmission unit 104 and sent to the transmission path. There is no problem if the low speed electric signal is other than STM-1, but here is described presuming STM-1. The memory capacity of the buffer memory unit 101 is reduced by using the reference clock and frame in the unit 1 inputted from the clock distribution unit 2 that are aligned to the frame phase of the STM-1 low speed electric signal and optionally delayed by setting from outside at the first variable delay unit 105 as the read clock and frame of the buffer memory unit 101.

At the receiving unit 200 the STM-n optical signal inputted from the transmission path is converted into the STM-n electric signal at the optical receiving unit 210, and frame synchronization is performed at the frame synchronization unit 220, and the overhead termination is performed for the STM-n electric signal at the overhead termination unit 230. At the demultiplexing unit 240 the STM-n electric signal is demultiplexed into N STM-1 signals according to the CCITT Recommendation G. 708, and transmitted to the pointer processing unit 250. The pointer processing unit 250 includes the pointer interpretation units 251-1 to 251-N, the memory units 252-1 to 252-N, the pointer operation units 253-1 to 253-N, and the pointer insertion units 254-1 to 254-N, and inputs N STM-1 signals in parallel from the demultiplexing

unit 240, and has a circuit of same configuration for each STM-1 signal. The STM-1 electric signal can be outputted from the high speed signal interface unit at optional phase as the read clock and frame of the memory unit 252-1 to 252-N of the pointer processing unit 250, by using the reference clock and frame in the unit 1 inputted from the clock distribution unit 2 that are set at optional phase by setting from outside at the second variable delay unit.

FIG.3 illustrates a frame format of an STM-1 signal. The signal rate of the STM-1 signal is 155.52Mb/S and the frame length is 19440 bits-(2430bytes). One frame consists of nine repetitions of a cycle T which consists of nine byte overhead portion and a payload portion (a framed data string having the transmission information from a terminal station). The leading nine-byte overhead of a one frame signal string includes a six byte frame synchronous signal (A1, A1, A1, A2, A2, A2), and the other nine byte overhead portion contains the information regulated in CCITT Recommendation G.708. In addition, the pointers (H1, H2, H3, each three bytes) are placed into the overhead of the fourth cycle T. The pointers indicate the number of data bits from the last bit of the pointers to the frame containing the leading position of payload frame. The receiving side can then detect the frame leading position in the payload by interpreting the pointers. As shown in FIG.3, where the payload follows immediately after the last bit of the pointers, the values of the pointers indicate the bit number from the leading bit of the payload to the frame containing the leading location of the data strings.

FIG.4 illustrates the pointer interpretation unit 251-1, the memory unit 252-1, the pointer operation unit 253-1 and the pointer insertion unit 224-1 in the pointer processing section 250. FIG.5 to FIG.7 are timing charts showing the operations of these components.

In FIG.4, the STM-1 signal, the clock signal and the frame synchronous pulse from the demultiplexing unit 240 are converted to a twenty-four bit parallel signal in the S/P (serial/parallel conversion) circuit 251. At this time, the bit rate of each parallel signal is slowed down to 6.48Mb/S (=155.52Mb/S÷24) as shown in FIG.5. The serial-parallel conversion starts when a frame synchronous pulse is inputted.

The pointer interpretation circuit 252 detects the location of the pointers H1, H2, H3 based on the parallel signal from the STM-1 signal. In the case of the STM-1 signal, it is easy to detect the pointer location because the number of bits the pointer is located from the frame synchronous pulse A1 - A3 is predetermined. The frame header(FH) generation circuit 253 detects the frames leading to the location of the data strings in the payload which follows H3 in the pointer overhead. This then generates the frame header pulse FH in the corresponding time slot. The frame header pulse FH is stored in the memory MEM and is read out by a reading clock pulse which is generated immediately after the storage operation.

The memory MEM has twenty-four 8 bit parallel-input/parallel-output FIFO memories or registers and can temporally store twenty-four parallel signals (refer to FIG.5) from the S/P circuit 251 in the corresponding MEM. This operation is performed by the writing clocks WLPS1 to WLPS8 from the writing clock generator 261 which are shown in FIG.6. While FIG.6 shows only one input of the twenty-four parallel signals, all of the twenty-four parallel signals are written in the twenty-four 8 bit parallel input/output memories by the writing clocks WLPS1 to WLPS8. The writing clocks WLPS1 to WLPS8 are not generated during the overhead (OH), but are repeatedly generated during the payload. Therefore, overhead OH is not stored in the memory MEM. Every cycle of the writing clocks WLPS1 to WLPS8 consists of 8bits, and generates while shifting by one bit. The memory MEM writes new data at every rising edge of WPLS1 to WPLS8. (The length in which the memory can store one bit is longer than the length of the overhead.)

The readout of the memory MEM is performed at a time when either of the reading clocks RPLS1 to RPLS8 from the reading clock generator 262 are at low levels. The reading clocks RPLS1 to RPLS8 generate in synchronization with the clock signal of the second variable delay unit 260. During the overhead period, the readout period (low level) extends as long as the length of the overhead. The overhead period appears at 90 bit cycle.

The pointer operation unit 253-1 has a counter which is reset to "0" just after detecting the location of the third H3 in the pointer overhead of each frame, as determined from the readout frame (the frame synchronous pulse of the variable delay unit 260). (Refer to FIG.7). When the frame header pulse FH is supplied from the MEM, the counter value (778), which shows the frame leading location of the payload, is inserted into the pointer insertion unit 254-1 (FIG.7 (b), (c)). The output of the pointer insertion unit 254-1 has no overhead other than the pointers (FIG.7(c)), but an overhead insertion circuit (not shown in Fig.1) inserts the required overhead at location which is reserved as shown in the memory output portion of FIG.6.

In Fig.1, the setting of delay quantity at the first variable delay unit 105 and the second variable delay unit 260 is divided into two. One is to set from outside of the unit 1 and the other is to set automatically within the unit 1. An embodiment of

setting delay quantity from outside is shown in Fig.8. The setting is performed with the terminals connected with the unit 1 from outside. A control signal from the terminals is received at the control interface unit 3, and the setting of delay quantity to the first variable delay unit 105 and the second variable delay unit 260 from the control interface unit 3 according to the control signal is performed.

An embodiment of automatically setting delay quantity within a synchronous optical multiplexing station is shown in Fig.9. Fig.9 shows an embodiment of configuration of a multiplexing terminal station.

The station comprises a working high speed signal interface unit 1-1 and a standby interface unit 1-2, a distribution unit 4, and N lower speed signal interface units 3-1 to 3-N. The high speed signal interface units 1-1 and 1-2 have the same structure as the unit 1 of Fig.1 except a unit 106 described hereinafter. Each the lower speed signal interface units 3-1 to 3-N is a terminal unit for terminating a lower channel signal of STM-1.

The distribution unit 4 includes an identification information insertion circuit 404, distribution circuit 401, selector 402 and buffer memory 403. The distribution circuit 401 distributes the outputs from the circuit 404 to the units 1-1 and 1-2. The selector 402 selects one of the outputs from the units 1-1 and 1-2. If the working unit 1-1 is down, the selector 402 selects the output of the standby unit 1-2. Buffer memory 403 synchronizes the output from the selector 402 with the clock signal supplied from the clock distribution unit 2.

The identification information insertion unit 404 inserts identification information into overheads of the STM-1 signals which is output from the lower speed signal interface units 3-1 to 3-N. At the high speed signal interface unit 1, the identification information in the STM-1 low speed signal supplied to identification information detection unit 106 is detected, and the setting of delay quantity to the first variable delay unit 105 and the second variable delay unit 260 is automatically performed based on the detected identification information.

Claims

1. A synchronous optical multiplexing station comprising a transmission unit for multiplexing N STM-m low speed signals of the SDH standard to an STM-n (n = N x m) high speed signal, and a receiving unit demultiplexing an STM-n high speed signal to N STM-m low speed signals, and having a clock distribution unit to generate a clock and frame pulse in a station based on a reference clock in the station, and distribute them to units in the system, wherein transmission unit having:
buffer memory unit means for aligning phases of N STM-m electric signals outputted from a slow speed signal interface unit and reading by a clock and frame in the station;
the first variable delay unit means for optionally varying a read frame phase of the buffer memory unit means for one frame by setting from outside with the frame phase of the STM-m electric signals inputted from the low speed signal interface unit;
multiplexing unit means for multiplexing N STM-m electric signals outputted from the buffer memory unit means to the STM-n electric signal according to the multiplexing rule of the SDH;
overhead insertion unit means for inserting an overhead into the STM-n signal outputted from the multiplexing unit means; and
optical transmission unit means for converting the STM-n electric signal in which the overhead is inserted to an STM-n optical signal and transmitting it to a transmission path;
said receiving unit having:
an optical receiving unit means for converting the STM-n optical signal inputted from the transmission path to the STM-n electric signal;
frame synchronization unit means for frame-synchronizing the STM-n electric signal;
overhead termination unit means for terminating the overhead of the frame-synchronized output signal of the frame synchronization unit means;
demultiplexing unit means for demultiplexing signals outputted from the overhead termination unit means to N STM-m electric signals;
pointer processing unit means for moving N STM-m signals from a transmission path clock and frame onto a clock and frame in the station, and modifying pointer information to show the practical leading point of the data within the STM-m signals to a value aligned to the frame in the station and sending out the signals to a low speed signal interface unit in the station as N STM-m electric signals;
the second variable delay unit means for optionally varying a frame phase for one frame by setting from outside at moving the clock and frame in the pointer processing unit means.

2. A synchronous optical multiplexing station as set forth in claim 1, characterized in that delay quantities of the first and second variable delay units means are set by receiving a control signal from outside through a control interface.

3. A synchronous optical multiplexing station as set forth in claim 1 or 2,characterized in that delay quantities of the first and second variable delay units means are set by inserting an identification information into the STM-m low speed signals by the slow speed signal interface unit, and detecting and identifying this at the high speed signal interface unit.

4. A synchronous optical multiplexing station as set forth in claim 1, 2, or 3, characterized in that the pointer processing unit means is equipped with a pointer interpretation unit, a memory unit, a pointer operation unit, and a pointer insertion unit.

5. A synchronous optical multiplexing station comprising a transmissision unit (100) composed of the buffer memory unit (101), a multiplexing unit (102), an overhead insertion unit (103), an optical transmission unit (104) and a first variable delay unit (105), wherein the receiving unit (200) is composed of an optical receiving unit (210), a frame synchronization unit (220), an overhead termination unit (230), a demultiplexing unit (240), a pointer processing unit (250) and a second variable delay unit (260), and a clock distribution unit (2), and wherein the read frame phase of the transmission side buffer memory unit is variable in the high speed signal interface unit and the read frame phases of the receiving side pointer processing unit by varying the reference clock and frame in the station inputted from the clock distribution unit (2) using the amount of delay of the first variable delay unit (105) and the second variable delay unit (260).

FIG. 1

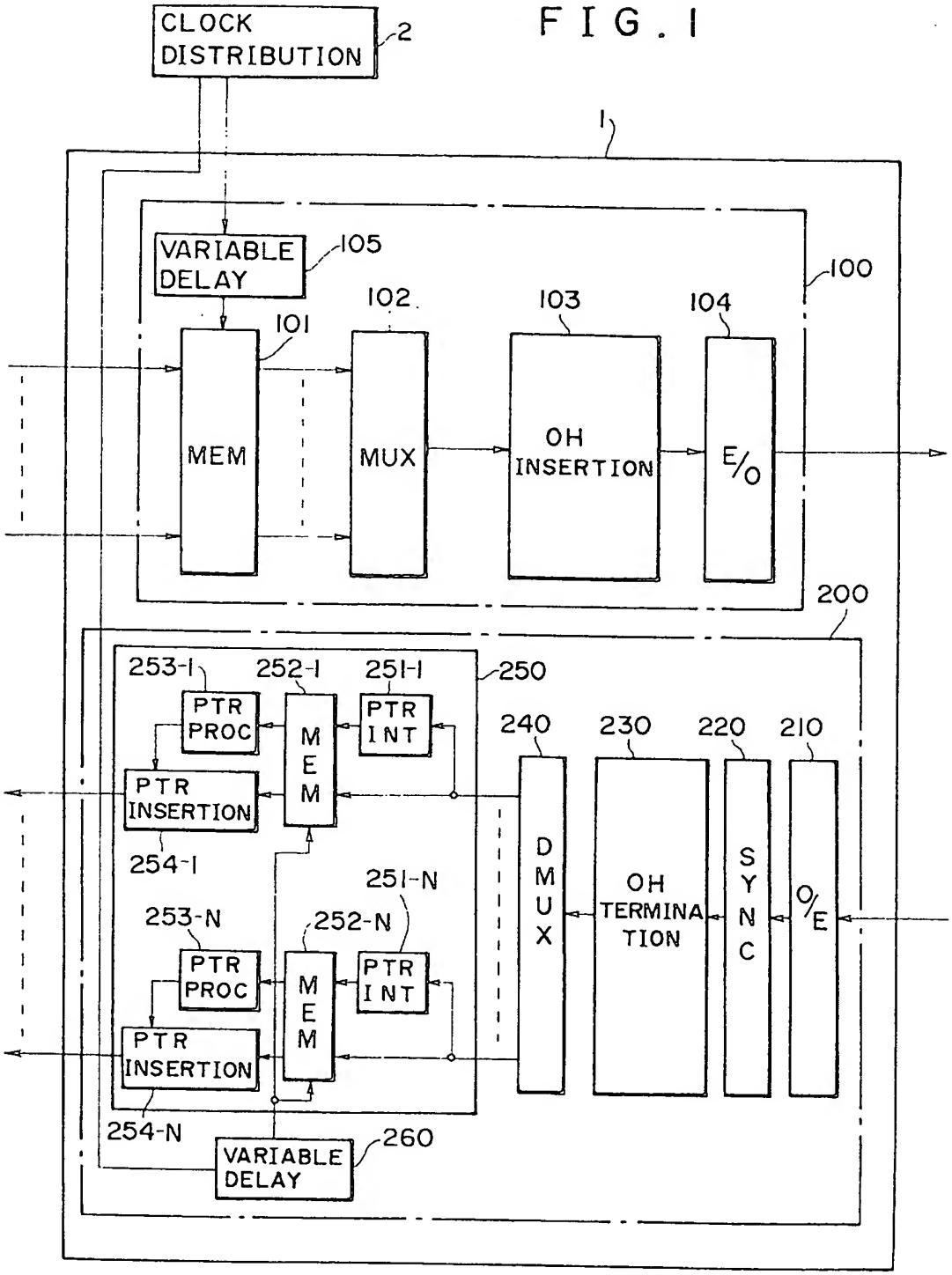
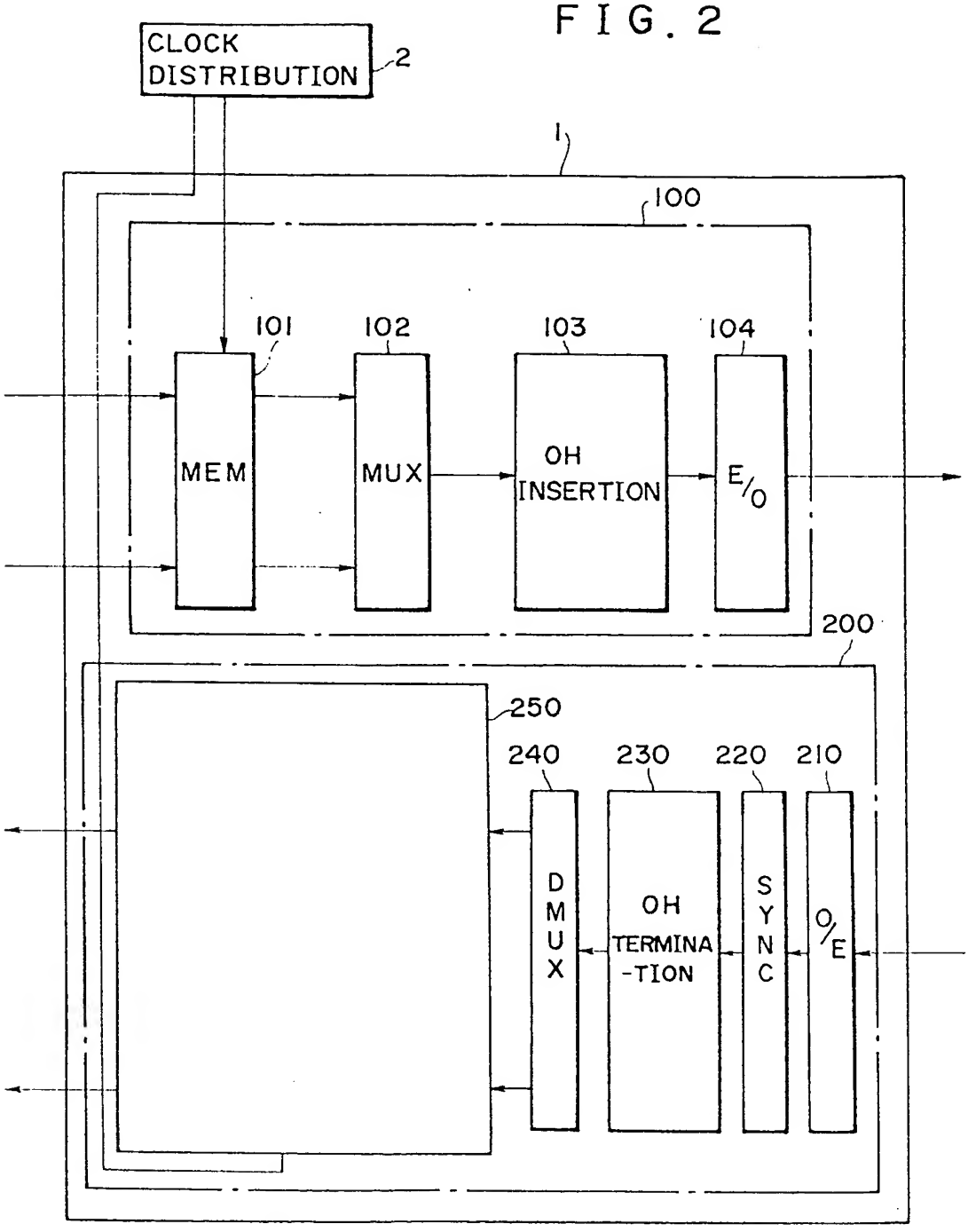

CLOCK DISTRIBUTION
2
1
VARIABLE DELAY
105
100
102
103
104
101
MEM
MUX
OH INSERTION
E/O
200
253-1
252-1
251-1
250
PTR PROC
MEM
PTR INT
240
230
220
210
PTR INSERTION
254-1
251-N
253-N
252-N
PTR PROC
MEM
PTR INT
PTR INSERTION
DMUX
OH TERMINATION
SYNC
O/E
254-N
VARIABLE DELAY
260

FIG. 2


CLOCK DISTRIBUTION
2
1
100
101
102
103
104
MEM
MUX
OH INSERTION
E/O
200
250
240
230
220
210
DMUX
OH TERMINA-TION
SYNC
O/E

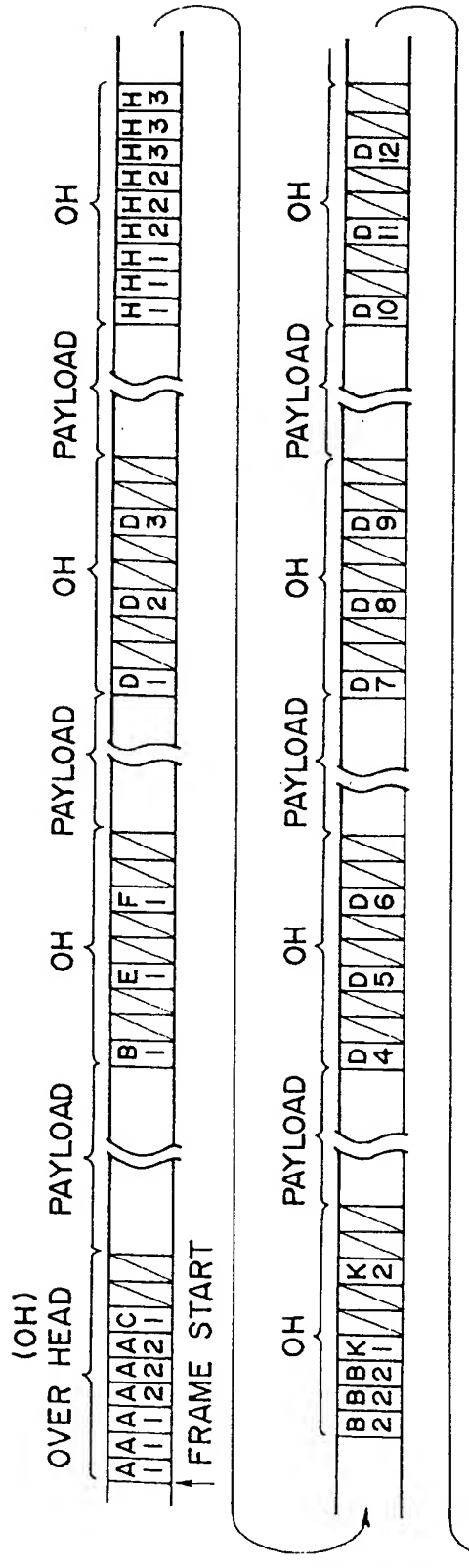
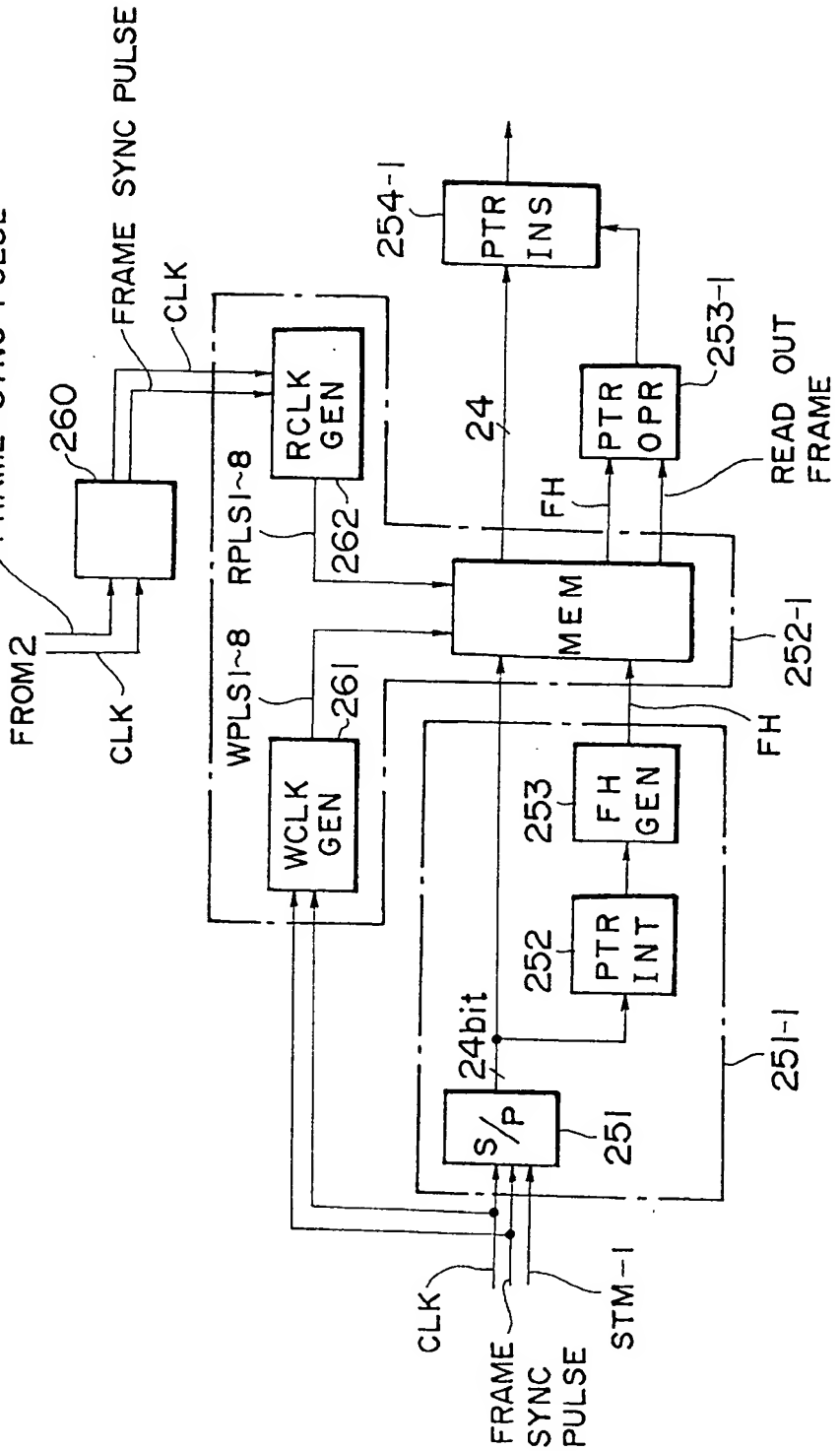


FIG. 3
FRAME FORMAT FOR STM-1

FIG. 4


FRAME SYNC PULSE
FROM2
CLK
260
FRAME SYNC PULSE
CLK
RCLK GEN
RPLS1~8
262
WPLS1~8
261
WCLK GEN
24
254-1
PTR INS
253-1
PTR OPR
READ OUT FRAME
FH
MEM
252-1
FH
253
FH GEN
252
PTR INT
24bit
S/P
251
251-1
CLK
FRAME SYNC PULSE
STM-1

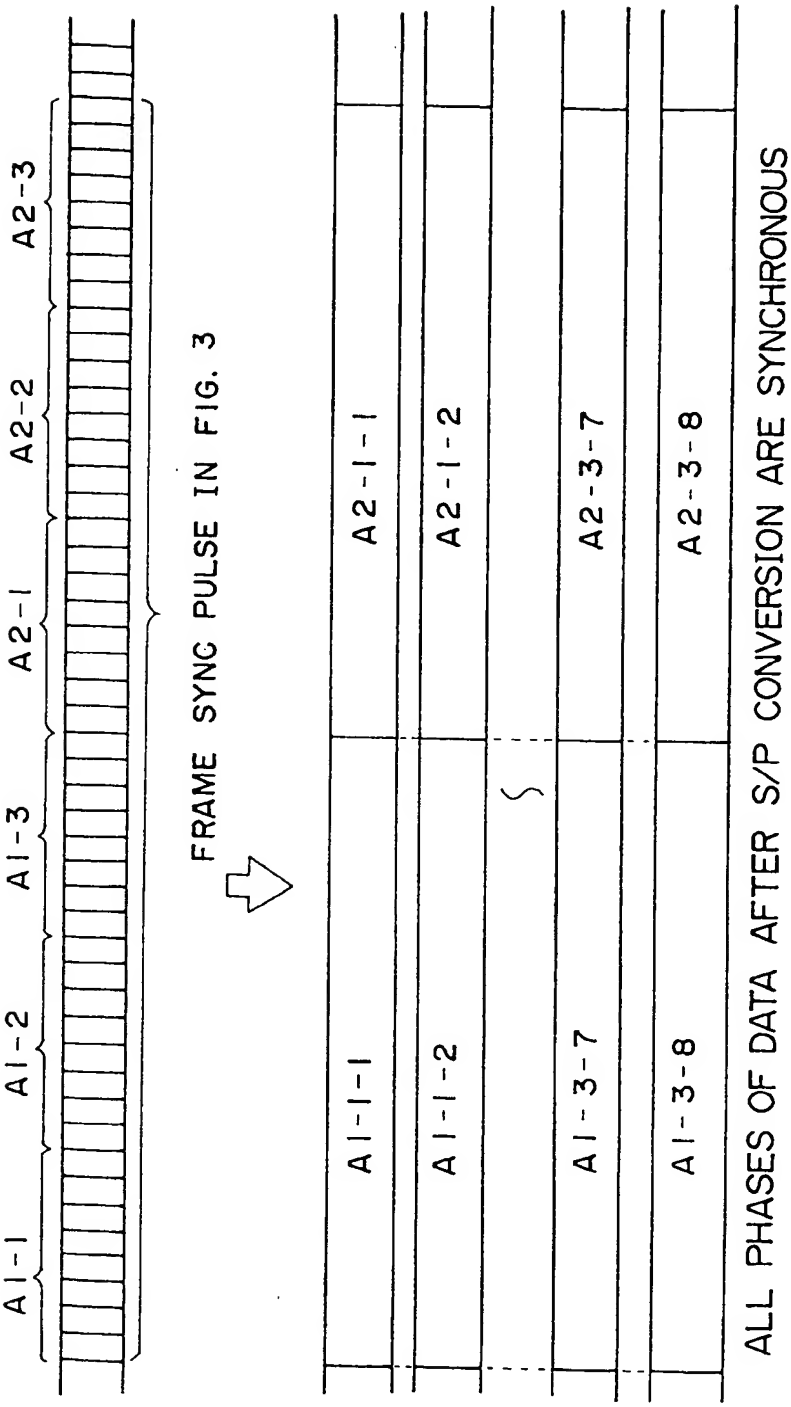


FIG.5
ONE DATA SELL INDICATES
ONE BIT FOR STM-1

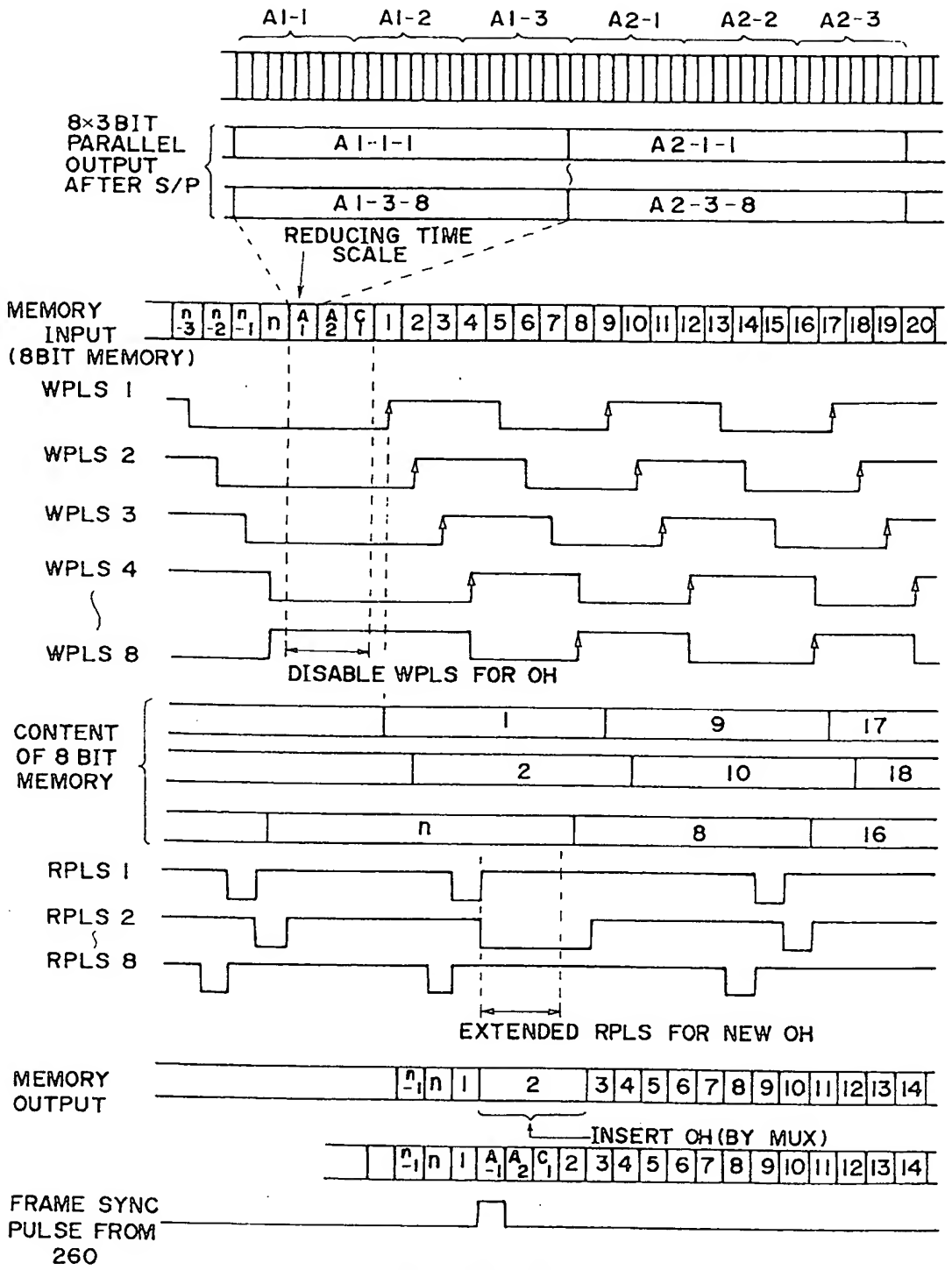
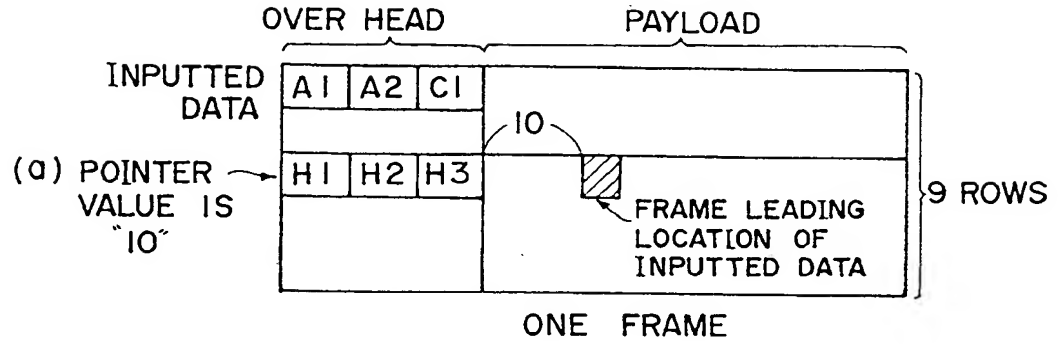
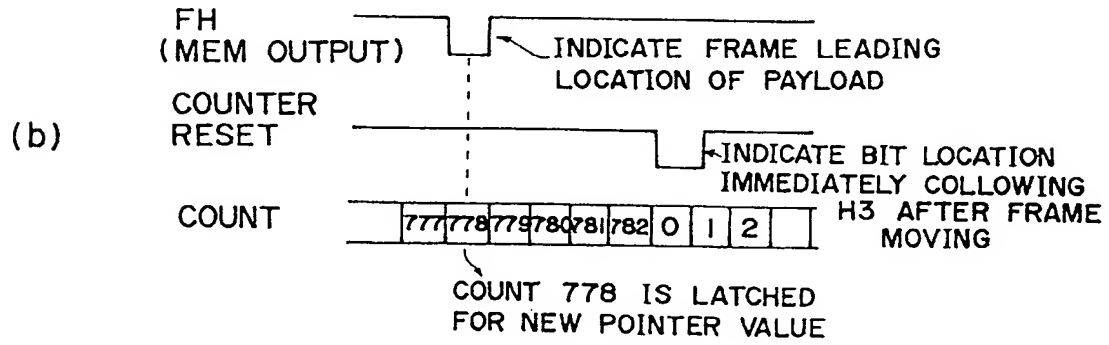


FIG.6
ONE DATA CELL INDICATES ONE BIT FOR STM-1

FIG. 7


OVER HEAD
PAYLOAD
INPUTTED DATA
A1
A2
C1
10
(a) POINTER VALUE IS "10"
H1
H2
H3
FRAME LEADING LOCATION OF INPUTTED DATA
9 ROWS
ONE FRAME


FH (MEM OUTPUT)
INDICATE FRAME LEADING LOCATION OF PAYLOAD
(b)
COUNTER RESET
INDICATE BIT LOCATION IMMEDIATELY COLLOWING H3 AFTER FRAME MOVING
COUNT
777
778
779
780
781
782
0
1
2
COUNT 778 IS LATCHED FOR NEW POINTER VALUE

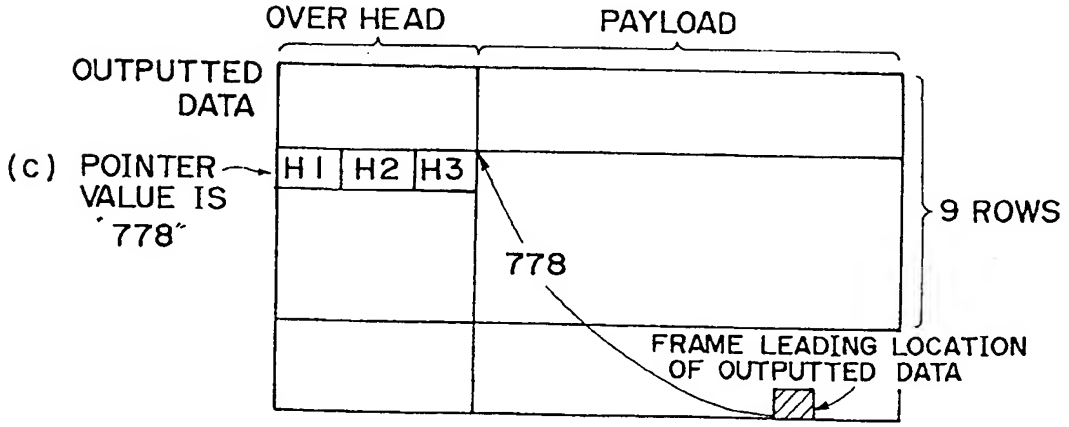

OVER HEAD
PAYLOAD
OUTPUTTED DATA
(c) POINTER VALUE IS "778"
H1
H2
H3
778
9 ROWS
FRAME LEADING LOCATION OF OUTPUTTED DATA

FIG. 8

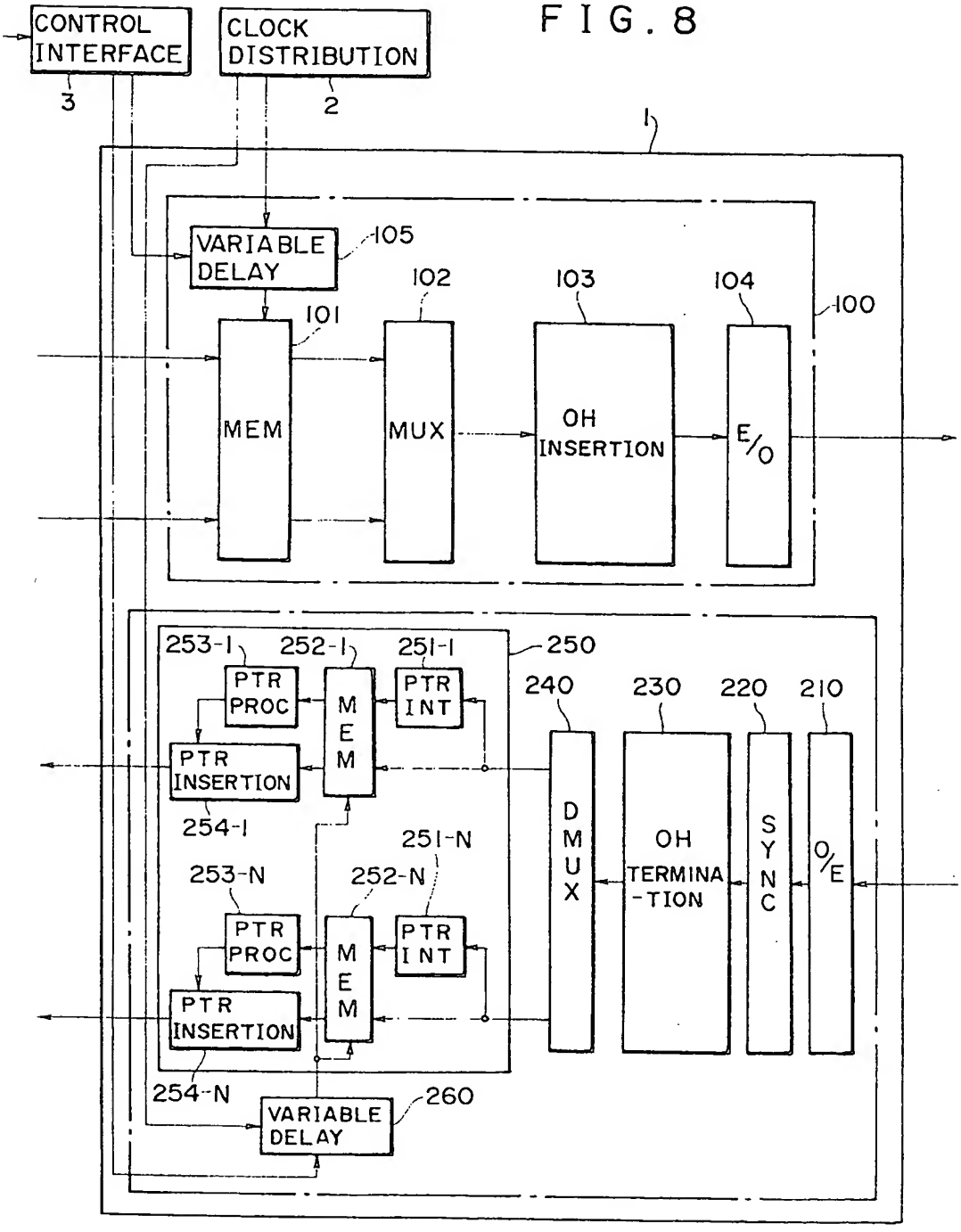
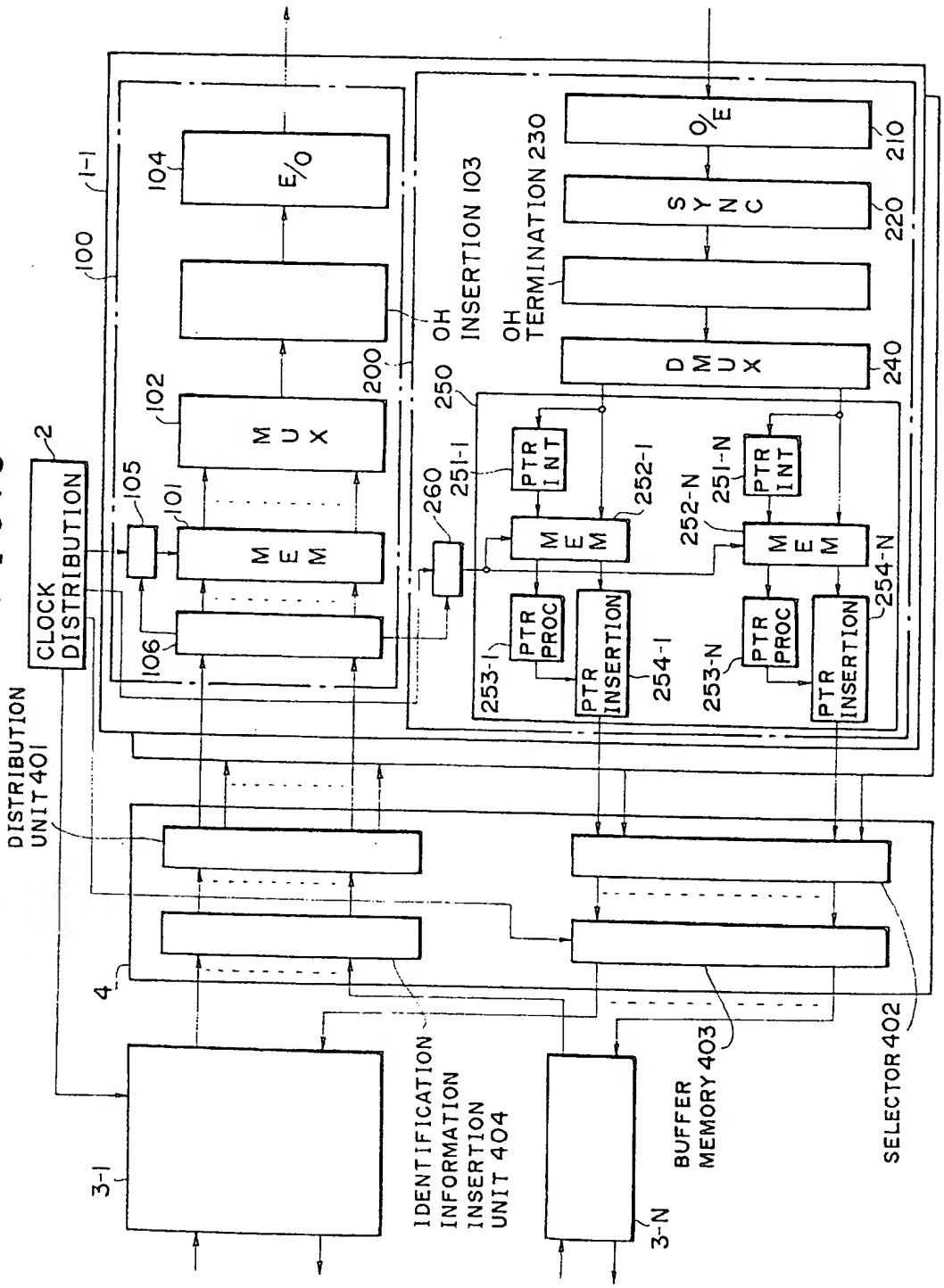

CONTROL INTERFACE
3
CLOCK DISTRIBUTION
2
1
VARIABLE DELAY
105
101
102
103
104
100
MEM
MUX
OH INSERTION
E/O
253-1
252-1
251-1
250
PTR PROC
M E M
PTR INT
240
230
220
210
PTR INSERTION
254-1
251-N
253-N
252-N
PTR PROC
M E M
PTR INT
PTR INSERTION
D M U X
OH TERMINA -TION
S Y N C
O/E
254-N
VARIABLE DELAY
260

FIG. 9


1-1
100
104
E/O
102
MUX
105
101
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European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 11 9608

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	PHILIPS TELECOMMUNICATION REVIEW vol. 49, no. 3, 1 September 1991, HILVERSUM NL pages 31 - 37 W. BUCHHOLZ ET AL. '2.5 Gbit/s SDH transmission at 1550 nm.' * page 33, column 1, line 1 - page 34, column 2, line 45 *	1-5	H04J3/16 H04J3/06
A	PROCEEDINGS IEEE INTERNATIONAL CONFERENCE ON COMMUNICATIONS vol. 2, 15 April 1990, ATLANTA (US) pages 381 - 390 H. KLINGER ET AL. 'A 2.4Gbit/s synchronous optical fiber transmission system.' * page 383, column 2, line 9 - page 384, column 1, line 36 *	1-5	
A	PROCEEDINGS OF THE NATIONAL COMMUNICATIONS FORUM vol. 44, no. 8/10, 1 October 1990, OAK BROOK, ILLINOIS US pages 131 - 136 GARY W. ESTER 'Sonet multivendor connectivity issues.' * page 132, column 1, line 6 - page 133, column 2, line 11 *	1-5	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H04J

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 FEBRUARY 1993	VAN DEN BERG J.G.J.

CATEGORY OF CITED DOCUMENTS

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